ON THE SWITCHING BEHAVIOUR OF A SINGLE PHASE CS PWM CONVERTER

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ABSTRACT - Switching behaviour of a Single Phase Current Source (CS) Pulse Width Modulation (PWM) converter with power reversal capability is presented. In one high frequency period, there are four switching subperiods. Among them, two are main subperiods and two are intermediate (transient) subperiods. Smooth operation of the converter requires appropriate snubber circuit across the DC link so as to protect the power electronic switches from high rate of voltage change. Results obtained from simulations and experimental model showed close agreement.

INTRODUCTION

Recent advancement in power seminconductor switches, open the door for the researchers to shift their interests into optimization of power processing methods. PWM techniques are the most widely used methods in the design of power processors. Before realizing a certain system, one has to work out all the details so that to ensure safe and reliable operation of such a system. Application of PWM in power processing overcomes a range of undisirable outcomes such as harmonics and poor power factor which are dominant in single pulse methods of power processing. On the other hand, PWM in power processing requires special care in designing the overall electronic switch module in order to avoid their damage under fast switching transients.

This paper presents a step by step switchig behaviour of a regenerative single phase delta modulated current source converter. The converter is a dual of a single phase current controlled hysteresis converter [1]. The non - regenerative three phase version is described in [2]. The stepwise principle of operation is explained in [2, 3]. Since the switching behaviour of the converter appears to be unique, this paper is devoted to present in detail, stepwise switching of the power electronic switches in the single phase bridge. A complete switching cycle of the bridge consists of four time intervals of which, two are main and the others are intermediate (transient). The paper is divided into three main parts. Part I briefly explains the principle of operation of the converter while part II describes the four switching time intervals of the converter giving the associated equations, and lastly the third part presents simulated and experimental results obtained from a transistorized laboratory model.

PART I: PRINCIPLES OF OPERATION

Details of the controls for the converter which are omitted in this paper may be obtained in [2,3]. Operation of the converter can best be described with the help of Figs. 1 and 2. Fig. 1 shows the power circuit of a single phase current source PWM rectifier. Fig. 2 shows the sketch of the waveforms of the ac side capacitor voltage, V_c which is kept within the set voltage tolerance and the dc link voltage, V_t.

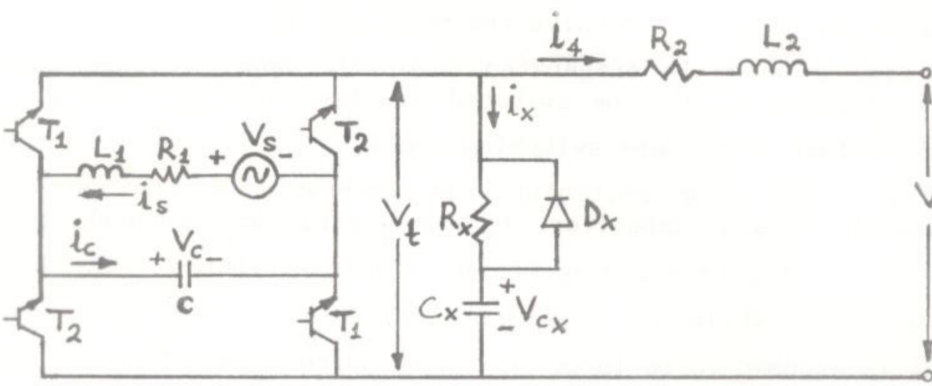


Fig.1 Single Phase CS PWM Converter

On the ac side the capacitor voltage is controlled to track the reference by charging and discharging the ac capacitor using the dc current. This is achieved by alternative switching of the power electronic switches T_1 and T_2. On the dc side the current is regulated using proportional control. The snubber circuit across the dc link is only important during transients, that is why it does not appear in outlining the principles of operation.

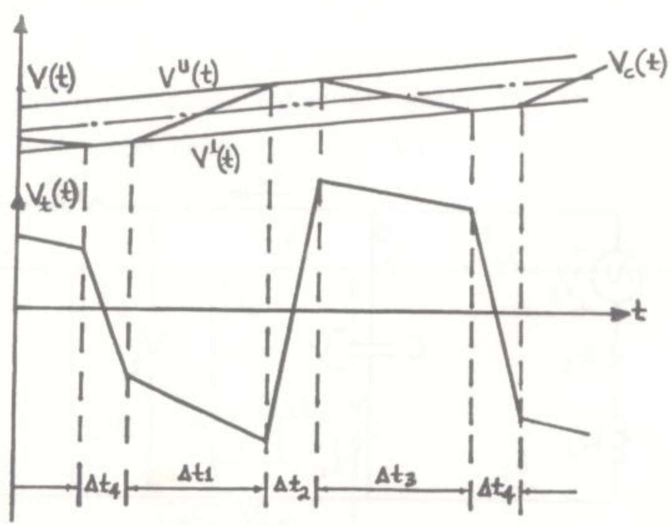


Fig.2 Waveforms of V^u, V^l, V_c and V_t with expanded time scale

PART II: SWITCHING TIME INTERVALS

In Fig. 1 the snubber circuit across the dc link consists of a Diode, D_x, Resistor, R_x and capacitor, C_x.

It is generally known that a transistor cannot turn on when the collector emitter is reverse biased, even if the base signal is applied. Furthermore, there is elapse of time between application of base signal and full response of the transistor (ON or OFF). For better understanding, a rising edge of the positive half cycle of the sinusoidal voltage source waveform is taken as a reference. In the bridge, the transistors with the same notation (T_1 or T_2) receive the same base drive signal.

Fig. 2 shows in exagerated form, the upper voltage bound V^u, the lower voltage bound V^l, the switched ac side capacitor voltage V_c and the DC link voltage V_t for one switching cycle.

There are four switching time intervals in one switching cycle: Charging the ac side capacitor (T_2 on, T_1 off), Δt_1, turning on T_1 while T_2 is still on, Δt_2, Discharging the ac side capacitor (T_1 on, T_2 off), Δt_3. Turning off T_1 while T_2 is already on, Δt_4. All the time, the DC link current is assumed to be large enough to supress the effect of an ac source current.

CHARGING THE AC SIDE CAPACITOR, Δt_1

Δt_1 is one of the main time interval during which the AC side capacitor is charged so as to raise its voltage from lower voltage bound to upper voltage bound.

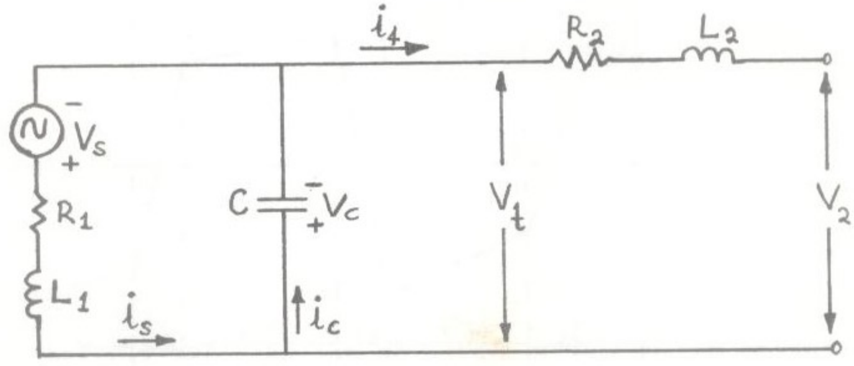


Fig.3 Charching the AC side capacitor, Δt_1: T_2 conducting

Fig.3 shows the equivalent circuit during Δt_1. At this stage the snubber circuit remains idle. The associated equations are given as

$$i_c = i_s + i_4 \tag{1}$$

But i_c can be expressed as

$$i_c = C\frac{dV_c}{dt} \tag{2}$$

Therefore equating the right hand sides of equations (1) and (2), we obtain equation (3) as

$$\frac{dV_c}{dt} = \frac{1}{C}\left(i_s + i_4\right) \tag{3}$$

From equation (3), it follows that

$$V_c = \frac{1}{C}\int\left(i_s + i_4\right)dt \tag{4}$$

From Fig.2 it can be seen that

$$V_c(t)\Big|_{\Delta t_1} = \frac{1}{C}\left(i_s + i_4\right)\Delta t_1 + V^l(t) \tag{5}$$

Also

$$V_{cx}(t) = -V_c(t)\Big|_{\Delta t_1} \approx -V^u(t) \tag{6}$$

TURNING ON OF T_1, Δt_2

This is intermediate time interval where T_1 transistor group is turned on while T_2 transistor group is turned off.

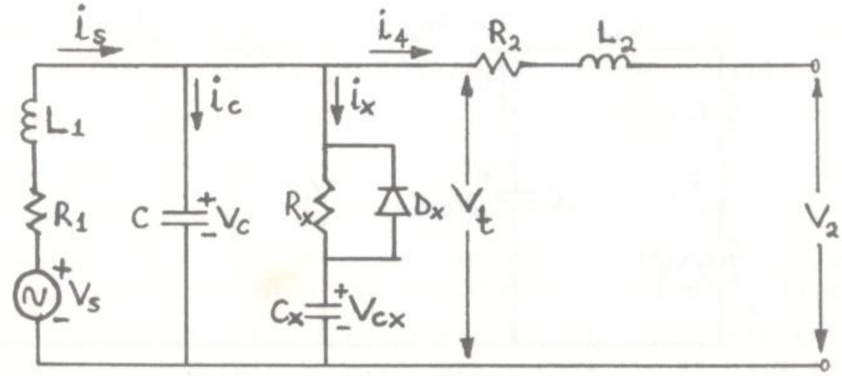


Fig.4 Turning on T_1 while T_2 is still on, Δt_2

Fig. 4 shows the equivalent circuit for the time interval Δt_2. When T_1 transistor group is turned on, T_2 transistor group will turn off automatically since they will be reverse biased. The AC source current will continue to charge the ac side capacitor while the DC link current will be reversing the direction of the snubber capacitor voltage V_{cx}. The corresponding equations during this interval will be

$$V_c(t) = V_{cx}(t) + i_x(t)R_x \tag{7}$$

where

$$i_x = C_x \frac{dV_{cx}(t)}{dt} \tag{8}$$

Therefore equation (7) could be rewritten into equation (9) as

$$V_c(t) = V_{cx}(t) + C_x R_x \frac{dV_{cx}(t)}{dt} \tag{9}$$

Solving this differential equation taking the initial conditions as given in eq. (6) we get

$$V_{cx}(t) = V^u(t)\left[1 - 2\exp(-\frac{t}{\tau_x})\right] \tag{10}$$

where

$$\tau_x = R_x C_x \tag{11}$$

DISCHARGING THE AC SIDE CAPACITOR, Δt_3

This is the other main time interval where the AC side capacitor is discharged to lower its voltage from upper voltage bound to lower voltage bound.

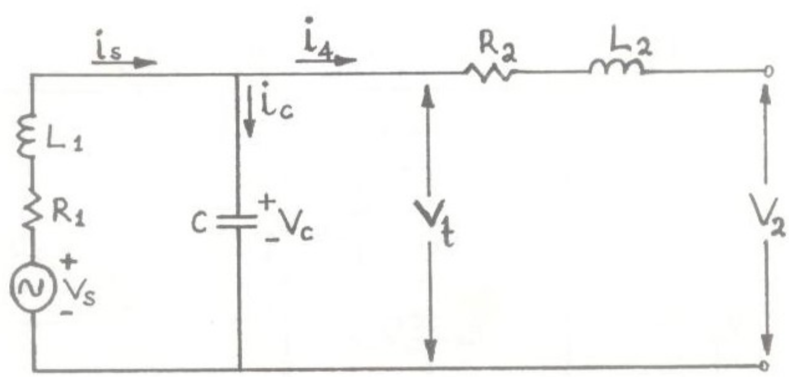


Fig.5 Discharging the AC side capacitor, Δt_3, T_1 conducting

Fig 5 shows the equivalent circuit during time interval Δt_3. The DC link current will be discharging the AC side capaci tor. At the same time power is transferred from the AC side to the DC link. The associated equations are given as:

$$i_c = i_s - i_4 \tag{12}$$

That is

$$\frac{dV_c}{dt} = \frac{1}{C}\left(i_s - i_4\right) \tag{13}$$

From which we get

$$V_c(t) = \frac{1}{C}\int\left(i_s - i_4\right)dt \tag{14}$$

Again, from Fig.2 it can be shown that

$$V_c(t)\Big|_{\Delta t_3} = \frac{1}{C}\left(i_s - i_4\right)\Delta t_3 + V^u(t) \approx V^l(t) \tag{15}$$

Also

$$V_{cx}(t)\Big|_{\Delta t_3} \approx V^l(t) \tag{16}$$

TURNING OFF T_1 (AFTER TURNING ON T_2), Δt_4

This is the intermediate time interval where T_1 transistor group is turned off while T_2 transistor group is already turned on. When T_2 transistor group is turned on while T_1 is still on, nothing will change since T_2 transistor group is reverse biased. But in order to avoid high rates of voltage changes across the bridge due to open circuit DC link, T_2 transistor group is turned on before T_1 group is turned off.

Fig. 6 shows the equivalent circuit for the time interval Δt_4. Before T_2 group is turned on, the snubber capacitor voltage, V_{cx}, should be equal or greater than the AC side capacitor voltage in the reverse direction so as to forward bias the transistors. During Δt_4 time interval the AC source current will be charging the AC side capacitor while the DC link current will be reversing the voltage across the DC link by opposite charging the snubber capacitor C_x.

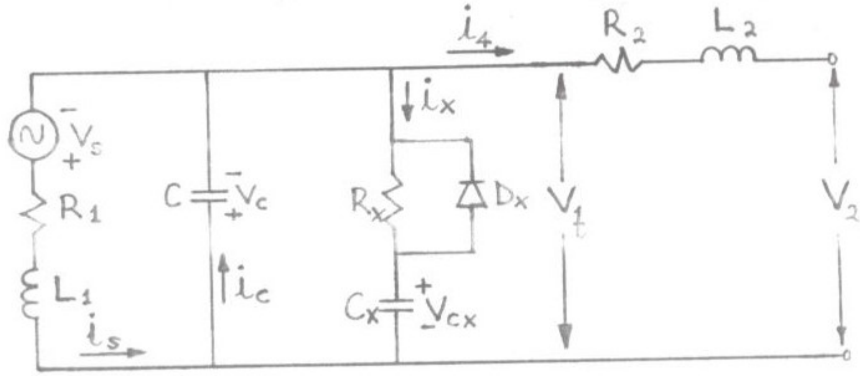


Fig.6 Turning off T_1 (after turning on T_2), Δt_4

The corresponding equations are given as

$$i_c = i_s = C\frac{dV_c}{dt} \tag{17}$$

And

$$\frac{dV_{cx}}{dt} = -\frac{i_4}{C_x} \tag{18}$$

At the end of time interval Δt_4 we have

$$V_{cx}(t)\Big|_{\Delta t_4} = -\frac{i_4 \Delta t_4}{C_x} + V^1(t) \tag{19}$$

At this moment

$$\left| V_c(t)\Big|_{\Delta t_4} \right| \le \left| V_{cx}(t)\Big|_{\Delta t_4} \right| \tag{20}$$

$$\left| -\frac{i_4 \Delta t_4}{C_x} + V^1(t) \right| \ge \left| V_c(t)\Big|_{\Delta t_4} \right| \tag{21}$$

The end of time interval Δt_4 is the start of time interval Δt_1 where the T_2 transistor group is fully on and both, AC source and DC link currents will be charging the AC side capacitor. During negative half cycle the switching sequence is reversed

PART III: RESULTS

In order to verify the theories given in part I of this paper, results from digital computer simulations are presented. The simulation results gave guide to the implementation of a 1kW practical model of the converter for checking switching behaviour.

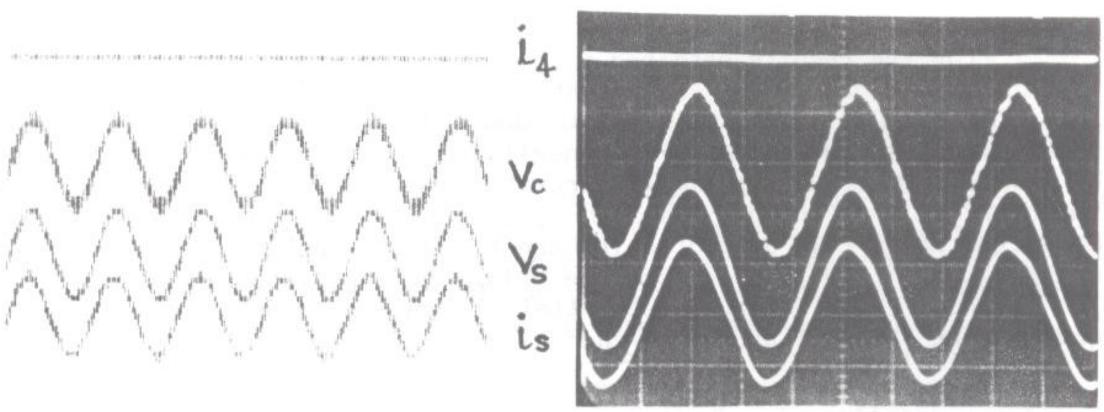
The parameters of the snubber circuit components used are:

D_x : 40HFL 60502, Recovery time 60 sec.

C_x : 4 μF, 400V

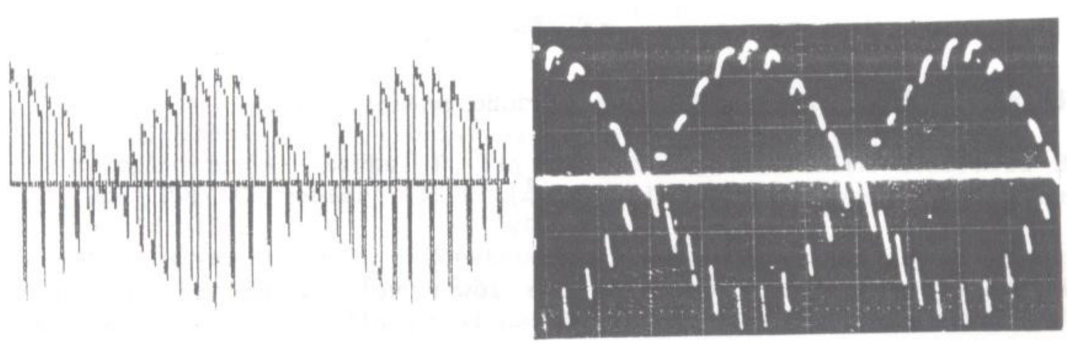
R_x : 10 Ω, 50W

Fig. 7 shows the simulated and experimentally obtained waveforms of DC link current, i_4, AC capacitor voltage, V_c, AC source voltage, V_s and AC source current i_s. Fig. 8 shows the simulated and experimentally obtained waveforms of the DC link voltage, V_t. Fig. 9 shows the simulated and experimentally obtained waveforms of the DC link voltage, V_t, with expanded time scale.



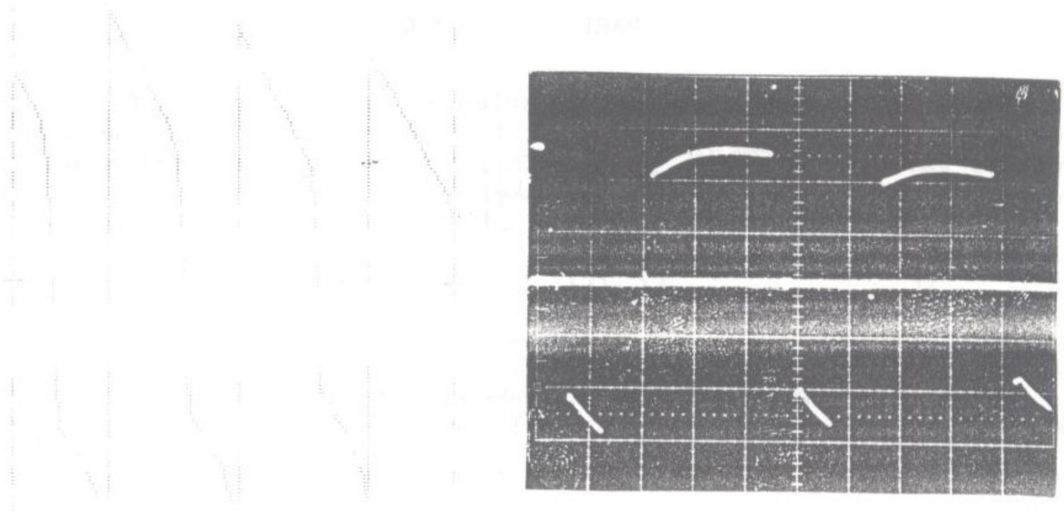
(a) (b)

Fig. 7 Typical waveforms (a) Simulated (b) Experimental



(a) (b)

Fig. 8 DC link voltage waveforms (a) simulated (b) experimental



(a) (b)

Fig.8 DC link voltage waveforms (a) simulated (b) experimental

From the results obtained from computer simulations and experiments, it can be seen that there is slight disagreement. This is due to the fact that the simulation results were obtained with an assumption that the ON/OFF times of the switches are negligible. However, from Fig. 8, it can be deduced that the snubber circuit across the bridge plays a very important role to ensure a smooth operation of the converter. The snubber capacitor has a role of protecting the bridge against high rates of voltage changes which take place across the bridge during switching instants.

From Fig. 2 it can be seen that the snubber capacitor voltage at the end of time interval Δt_4 is given by

$$V_{cx}(t)\Big|_{\Delta t_4} = -V^1(t) \qquad (22)$$

Equating eqs. (19) and (22) can be combined to yield eq.(23)

$$-\frac{i_4 \Delta t_4}{C_x} + V^1(t) = -V^1(t) \qquad (23)$$

Therefore the value of C_x should be chosen such that

$$C_x \geq \frac{i_4 \Delta t_4}{2\hat{V}^1} \qquad (24)$$

Where $\hat{V}^1$ is the peak value of the lower voltage bound. If the voltage tolerance is made small, eq. (24) can be simplified to yield eq. (25)

$$C_x \geq \frac{i_4 \Delta t_4}{2\hat{V}} \qquad (25)$$

where $\hat{V}$ is the peak reference voltage. It is important to note that each intermediate time intervals Δt_2 and Δt_4 should not be less than the total response time of the power electronic switches in the bridge. That is

$$\Delta t_2 \geq t_{on_1} + t_{off_2} \quad (26)$$

$$\Delta t_4 \geq t_{on_2} + t_{off_1} \quad (27)$$

where t_{on_1} is the time required for T_1 transistor group to turn on, t_{on_2} is the time required for T_2 transistor group to turn on, t_{off_1} is the time required for T_1 transistor group to turn off and t_{off_2} is the time required for T_2 transistor group to turn off. Under ideal conditions, equations (26) and (27) yield equation (28).

$$\Delta t_2 \approx \Delta t_4 \quad (28)$$

CONCLUSIONS

Step by step analysis of the switching behaviour of a single phase CS PWM converter gives a guide for the dimensioning of the single phase bridge snubber circuit. The snubber circuit is necessary for protection of the valves from high rate of voltage change. Results from simulations and experiments showed close agreement to those obtained analytically. From analytical results (eqn.25) it can be deduced that the snubber capacitor should be chosen in such a way that the rate of voltage change across the bridge is less than the rated value of the electronic switches constituting the bridge.

REFERENCES

[1] Stihi, O. "Single Phase Current Controlled Hysteresis Converter" M.Eng. thesis, McGill University, July, 1986.

[2] Mwinyiwiwa, B., Birks, P. P. and Ooi, B. T. "Delta Modulated Buck Type PWM Converter" IEEE Ind. Appl. Society Annual Conference Record, 1989.

[3] Mwinyiwiwa, B. M.M. "Construction and Test of a 3 Phase Delta Modulated Buck type PWM Converter", M.Eng. thesis, McGill University, July, 1989.