THE USE OF HARD AND SOFT DECISIONS IN FRAME SYNCHRONIZATION.

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Abstract

In many frame synchronized systems, the receiver bases synchronization on *hard decisions*, in which the received markers are not allowed to have any mismatches from the transmitted ones. Some studies, however, have shown that by allowing a certain degree of mismatch, thereby creating *soft decisions*, the performance of the systems can be improved. This report goes on to propose a strategy of applying both *hard* and *soft decisions* which gives better performance than one reported elsewhere. Optimum design parameters that incorporate the proposed *hard* and *soft decision* strategy are also presented.

INTRODUCTION

In communication systems employing frame synchronization, special sequences of bits called markers are inserted in the transmitted bit-stream. Such markers enable the receiver to identify where the data occurs in the bit-stream as well as to keep the receiver synchronized to the transmitter. In order for the communication system to operate properly, the receiver must search for the markers in the received bit-stream each time it loses synchronization, and it must try to maintain the synchronization once established. Unfortunately, when instabilities and noise increase in the channel, a lot of the transmitted bits are received in error, and the receiver fails to locate the markers correctly, thus leading to the loss of a lot of data. In order to combat this problem, a lot of studies aimed at investigating the behaviour of frame synchronized systems have been undertaken. Most of these studies have focused on the receiver, because it is the receiver which has to process both data and markers that have been corrupted in the channel.

Some of the studies undertaken on the receiver have shown that proper bit sequences must be chosen for the markers in order for the communication systems to attain acceptable performance [1,2]. The first strategy for improving the performance of the systems has therefore been to choose markers with appropriate bit sequences [1,2,3]. Other studies have shown that, by verifying the correctness of the marker each time the receiver is recovering from loss of synchronization or is about to lose synchronization, then the performance of the systems can be improved dramatically [4,5]. The second strategy has therefore been to determine the number of such verifications, both during synchronization recovery and during loss of synchronization [5,6]. The proposed bit sequences for the markers, the number of verifications during synchronization recovery, and the number of verifications during loss of synchronization form the optimum design parameters in frame synchronized communication systems.

Some of the optimum design parameters proposed for frame synchronized communication systems have been adopted as international standards [7]. Due to developments in communication technology, however, alternative parameters having better performance have been continuously proposed. For example, in 1980, a receiver which was able to lower the recovery time of PCM systems from 43 ms to 29 ms was proposed [8]. Later on, another receiver capable of lowering the time needed to detect loss of synchronization by a factor of 4 was also proposed [9]. Other proposed schemes for such

systems include the one by Dodds [10], which decreased the reframe time from 48 ms to 3 ms and raised the maintenance time from 1.9 s to 8.5 centuries, and the one by Driessen [11], which led to improved synchronization reliability. Recently, new optimum design parameters showing improved performance over the G.732, G.742, G.745 and G.751 CCITT schemes have been proposed [12].

Another addition to the optimum design parameters arises from the technique of accepting received markers as valid even when they contain some errors. This technique has received considerable attention, because studies have shown that the performance of the systems can be improved considerably by its application [6,10]. This then gives rise to the third strategy for improving the performance of the *hard decision* (no errors allowed) schemes recommended by CCITT [7] by allowing some kind of *soft decision* (some errors allowed). In this report, the technique of applying both *hard* and *soft decisions* in frame synchronization is investigated. First, the performance expressions for two such systems are derived. The performances of the two systems are then compared, and the corresponding optimum design parameters for the system showing better performance derived. The measure of performance used in the analysis is the synchronization efficiency, although the recovery and holding times are also used for comparison with systems reported elsewhere.

SYSTEM MODEL AND ANALYSIS

The two types of systems analyzed in this report are referred to as strategy A and strategy B. Both of them are based on the same receiver configuration whose transition diagram is given in Fig. 1, and which has the following characteristics. It has the usual true (1, 2, 4, 6) and false (1, 3, 5, 7) paths; it has the usual recovery verify number (N) and loss verify number (M), both of which are 2 in this case; its operation in the false path is exactly the same as that in the true path; and, transitions between its states are governed by the number of mismatches (u) between a received word and the error-free marker.

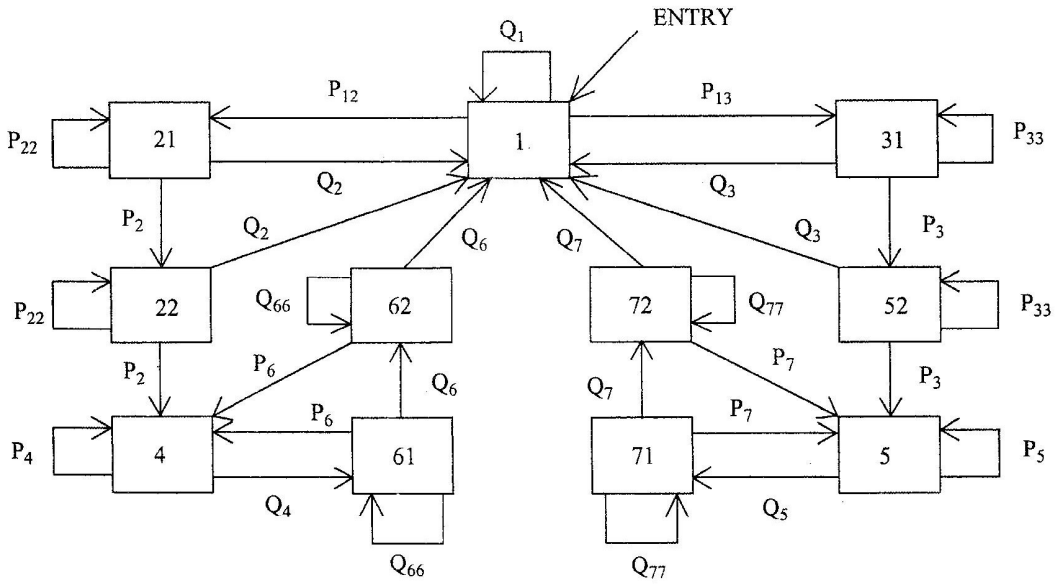

Figure 1: Transition diagram of the receiver with N = M = 2.

Following the true path, the receiver employing strategy A operates as follows. Once in state 1, it remains there as long as $u > u_1$ (Q_1) but advances to state 2 otherwise. Once in state 2, it remains there as long as $u_1 < u \leq u_2$ (P_{22}), but advances towards state 4 if $u \leq u_1$ (P_2) or returns to state 1 if $u > u_2$ (Q_2). Once in state 4, it remains there as long as $u \leq u_3$ (P_4) but advances towards state 1 if $u > u_3$ (Q_4, Q_6). However, it remains in state 6 as long as $u_4 < u \leq u_3$ (Q_{66}), but returns to state 4 if $u \leq u_4$ (P_6). The receiver employing strategy B operates like that of strategy A in the synchronization recovery phase. However, once in state 4, it remains there as long as $u \leq u_3$ (P_4) but advances to state 6 if $u > u_3$ (Q_4). Once in state 6, it remains there as long as $u_3 < u \leq u_4$ (Q_{66}), but advances towards state 1 if $u > u_4$ (Q_6) or returns to state 4 if $u \leq u_3$ (P_6). As mentioned before, operation in the false path resembles that in the true path. Also, note that the receiver employing strategy B resembles the one analyzed by Jones and Al-Subbagh [6].In order to compute the transition probabilities shown in Fig. 1, first note that the communication system uses frames of length FL bits of which S are marker and FL-S are data bits. Next, note that when mismatches are allowed in the marker, the transition probabilities can be given by (2) in [1]. However, using our notations, we refer to a sequence of S bits as a word. Now, if the received word consists of S-R marker bits and R data bits; and if the Hamming distance between the transmitted S-R marker bits and the receiver S-R test bits is h; and the allowed error threshold in the marker is u bits; then the probability that the received word matches the error-free marker within the error threshold is given by

$$P(S,\ R,\ h,\ u) = \left.\begin{aligned} &\sum_{v=0}^{\min(u,\,S-R)} \sum_{j=\max(0,\,v-h)}^{\min(v,\,S-R-h)} \binom{S-R-h}{j}\binom{h}{v-j}(1-P_e)^{S-R-h+v-2j} P_e^{h-v+2j} \\ &\qquad x\ \frac{1}{2^R} \sum_{k=0}^{\min(u-v,\,R)} \binom{R}{k} \end{aligned}\right\} \tag{1}$$

where P_e is the probability of receiving a transmitted bit in error. This result can then be used to obtain the transition probabilities in Fig. 1. For example, for the receiver employing strategy A, if the received word is the marker, then

$$P_2 = P(S,0,h,u_1) = \sum_{v=0}^{\min(u_1,S)} \sum_{j=\max(0,v-h)}^{\min(v,S-h)} \binom{S-h}{j}\binom{h}{v-j}(1-P_e)^{S-h+v-2j} P_e^{h-v+2j} \tag{2}$$

and if it consists of both marker and data bits, then

$$P_3 = P(S,R,h,u_1) = \left.\begin{aligned} &\sum_{v=0}^{\min(u_1,S-R)} \sum_{j=\max(0,v-h)}^{\min(v,S-R-h)} \binom{S-R-h}{j}\binom{h}{v-j}(1-P_e)^{S-R-h+v-2j} P_e^{h-v+2j} \\ &\qquad x\ 2^R \sum_{k=0}^{\min(u_1-v,R)} \binom{R}{k} \end{aligned}\right\} \tag{3}$$

whereas if it consists of data bits only, then

$$P_3 = P(S,u_1) = \frac{1}{2^S} \sum_{k=0}^{\min(u_1,S)} \binom{S}{k}. \tag{4}$$

In order to obtain the performance expressions for the receiver, note that only a little modification is needed on those given in earlier reports. Therefore, the recovery time through the true path, the recovery time through the false path, the holding time through the true path and the holding time through the false path as given by (22), (23), (24) and (25) respectively in [5] become

$$L_{14} = \left[\left\{ \alpha + \frac{P_{12}\left[(1-P_{22})^N - P_2^N\right]}{(1-P_{22}-P_2)(1-P_{22})^N} + \frac{P_{13}\left[(1-P_{33})^N - P_3^N\right]}{(1-P_{33}-P_3)(1-P_{33})^N} \right\} \right.$$

$$\left. + \frac{P_{13}P_3^N}{(1-P_{33})^N} \left\{ \frac{(1-Q_{77})^N}{Q_5 Q_7^M} + \frac{\left[(1-Q_{77})^M - Q_7^M\right]}{(1-Q_{77}-Q_7)Q_7^M} \right\} \right] \Big/ \left[\frac{P_{12}P_2^N}{(1-P_{22})^N} \right] \tag{5}$$

$$L_{15} = \left[\left\{ \alpha + \frac{P_{12}\left[(1-P_{22})^N - P_2^N\right]}{(1-P_{22}-P_2)(1-P_{22})^N} + \frac{P_{13}\left[(1-P_{33})^N - P_3^N\right]}{(1-P_{33}-P_3)(1-P_{33})^N} \right\} \right.$$

$$\left. + \frac{P_{12}P_2^N}{(1-P_{22})^N} \left\{ \frac{(1-Q_{66})^M}{Q_4 Q_6^M} + \frac{\left[(1-Q_{66})^M - Q_6^M\right]}{(1-Q_{66}-Q_6)Q_6^M} \right\} \right] \Big/ \left[\frac{P_{13}P_3^N}{(1-P_{33})^N} \right] \tag{6}$$

$$L_{41} = \left[\frac{(1-Q_{66})^M}{Q_4 Q_6^M} + \frac{\left[(1-Q_{66})^M - Q_6^M\right]}{(1-Q_{66}-Q_6)Q_6^M} \right] \tag{7}$$

and

$$L_{51} = \left[\frac{(1-Q_{77})^M}{Q_5 Q_7^M} + \frac{\left[(1-Q_{77})^M - Q_7^M\right]}{(1-Q_{77}-Q_7)Q_7^M} \right] \tag{8}$$

Likewise, for the synchronization efficiency, the times needed to process one bit when the receiver fails to reach the true sync state are given by (15) and (16) in [2]. In this analysis, these then become

$$L_{18}(L) = \alpha + P_{12}\left[\frac{1}{(1-P_{22}-P_2)} - \frac{P_2^N}{(1-P_{22}-P_2)(1-P_{22})^N} - \left\{ \alpha + \frac{N}{(1-P_{22})} \right\} \frac{P_2^N}{(1-P_{22})^N} \right] \tag{9}$$

and

$$L_{18}(l)=\left[\left\{\alpha+\frac{P_{13}\left[(1-P_{33})^N-P_3^N\right]}{(1-P_{33}-P_3)(1-P_{33})^N}\right\}+\frac{P_{13}P_3^N}{(1-P_{33})^N}\left\{\frac{(1-Q_{77})^M}{Q_5Q_7^M}+\frac{\left[(1-Q_{77})^M-Q_7^M\right]}{(1-Q_{77}-Q_7)Q_7^M}\right\}\right]. \quad (10)$$

For the other parameters, we obtain

$$\left.\begin{aligned} T_l &= \sum_{l=1}^{L-1} L_{18}(l) \\ T_p &= T_l + L_{18}(L) \end{aligned}\right\} \quad (11)$$

and

$$\left.\begin{aligned} T_m &= (T_l + L_{14} - (\alpha + N))T_p \\ T_o &= T_m + (\alpha + N) \\ T_s &= l + L_{41} \end{aligned}\right\} \quad (12)$$

with the synchronization efficiency given by

$$\eta = \frac{T_s}{T_s + T_o} \quad (13)$$

RESULTS AND DISCUSSION

The obtained performance expressions can now be used to make various comparisons. In the following results, L stands for the frame length FL in bits with $FL = 2^L$, S for the marker length, N for the recovery verify number, M for the loss verify number, E for the error rate ($P_e = 10^{-E}$), L_{14} for the recovery time through the true path, L_{15} for the recovery time through the false path, L_{41} for the holding time through the true path and L_{51} for the holding time through the false path. First, we compare CCITT G.751 ($u_1 = u_2 = u_3 = u_4 = 0$), strategy A ($u_1 = 0$, $u_2 = u_3 = 1$, $u_4 = 0$), and strategy B ($u_1 = 0$, $u_2 = 1$, $u_3 = 0$, $u_4 = 1$). Using $L = 8$, $S = 8$, $N = M = 1$ and $E = 3$ the synchronization efficiencies for these schemes are 0.9981, 0.999999998 and 0.9999993 respectively. We therefore see from these results that allowing some kind of *soft decision* ($u > 0$) in detecting the marker increases the performance of the system. A similar conclusion was also drawn by Al-Subbagh and Jones [6]. Next we compare strategies A and B. The results for this comparison are given in Figs. 2-4. In these results, unless indicated otherwise, the system parameters have been set to $L = 8$, $S = 8$, $N = M = 1$, $E = 2$, $u_1 = 0$ and $u_2 = 1$. Also u_3 and u_4 have been set to 1 and 0 respectively in strategy A and 0 and 1 in

strategy B. In Fig.2, we first note that the synchronization efficiency decrease with u_1 for both strategies (with u_2 set to 7). Secondly, we note that strategy A has better performance than strategy B. In Fig. 3, we also note that the sychronization efficiency decrease with u_2 for both strategies, but strategy A has better performance than strategy B.

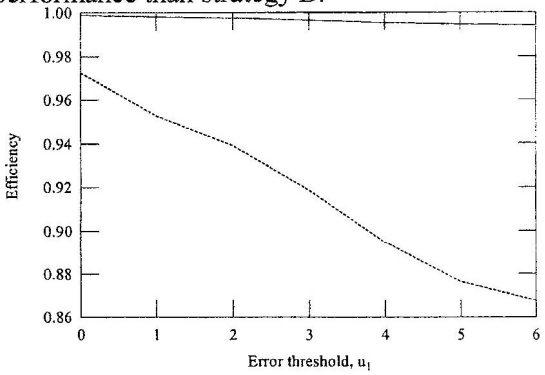

Figure 2: Efficiency versus threshold u_1 for strategy A (——) and B (·····).

Attempts to investigate performance with one of u_3 or u_4 varying and the other being held constant did not give easily discernible results, although the synchronization efficiency was found to increase with both u_3 and u_4. A better picture was therefore obtained by allowing both u_3 and u_4 to vary. Consequently, we have set $u_4 = u_3 - 1$ in strategy A and $u_3 = u_4 - 1$ in strategy B in Fig. 4. It can therefore be seen from the combined effects of both u_3 and u_4 that the synchronization efficiency increases with both u_3 and u_4. It is also observed, however, that strategy A has better performance than strategy B.

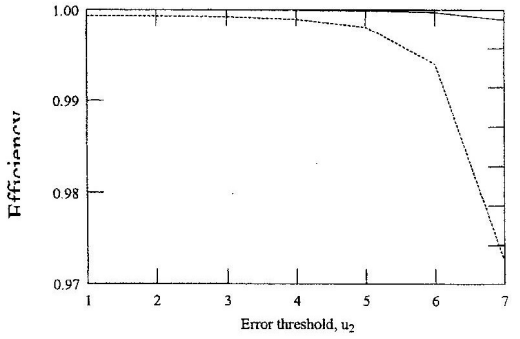

Figure 3: Efficiency versus threshold u_2 for strategy A (——) and B (·····).

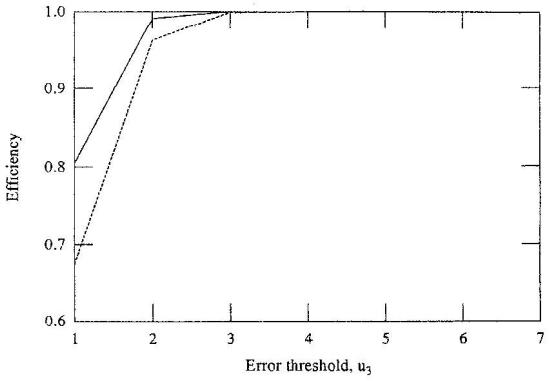

Figure 4: Efficiency versus threshold u_3 for strategy A (——) and B (·····).

The obtained results have shown that strategy A has better performance than strategy B. Consequently, only the optimum design parameters for strategy A are computed. In computing these parameters, we are tempted to use lower values of both u_1 and u_2 and higher values of both u_3 and u_4. This is due to the fact that the results of Figs. 2-4 show that such a choice promises higher system efficiencies. However, if we observe the results of Fig. 5 we are tempted to think otherwise because the recovery time increases with u_3. Although it is not shown, the recovery time was also found to increase with u_4. Consequently, we are cautioned to use lower values of both u_3 and u_4. In Fig. 6, however, the holding time increases with u_3 (and also with u_4 although it is not shown), again providing a temptation to use higher values of both u_3 and u_4. The contradiction here arises from the fact that the synchronization efficiency gives the relative amount of recovered to lost data but does not give the actual amount of recovered or lost data. The actual amount of lost data (in frames) is given by the recovery time and the recovered data by the holding time. Therefore, in choosing the optimum design parameters for the system, the synchronization efficiency does not suffice as the sole criteria. Consequently, the computed parameters have been based on high efficiency, high holding time and low recovery time. We point out that no contradictions were found in both the recovery and holding times with regard to either u_1 or u_2.

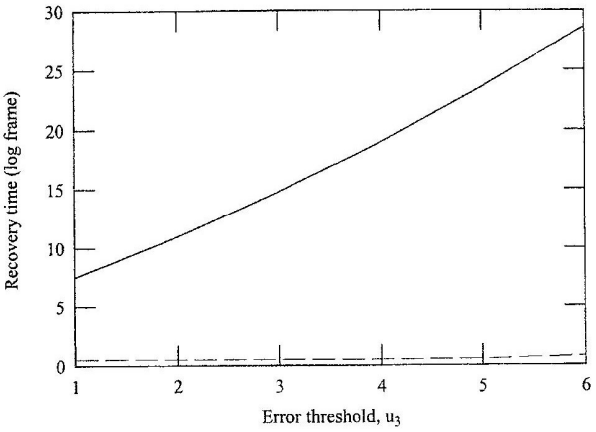

Figure 5: Recovery time versus threshold u_3 for true (——) and false (— —) paths.

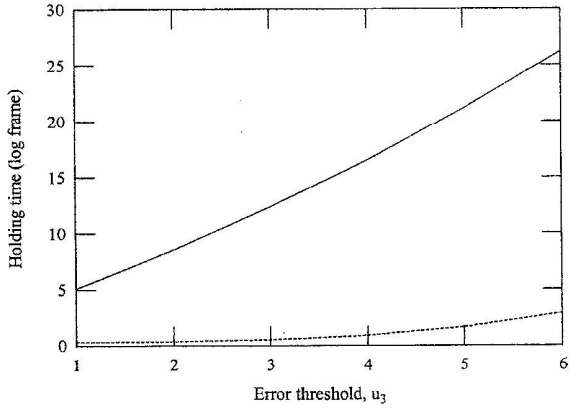

Figure 6: Holding time versus threshold u_3 for true (——) and false (— —) paths

The computed design parameters for systems employing frame lengths of 16 ($L = 4$) to 16384 ($L = 14$) bits are given in Table 1. These were computed to meet the following performance requirements: worst case error rate of $P_e = 10^{-2}$ ($E = 2$), minimum efficiency of 0.999999, $L_{15} >$ 3.0E+11*L_{14}, $L_{41} >$ 3.0E+13*L_{51}, and minimum recovery time on loss of synchronization. Note that with these requirements, if frames of 125 μs are used, then the receiver will take 1 year to reach the sync state through the false path compared to only 125 μs through the true path, and it will take 1 century to lose synchronization through the true path compared to only 125 μs through the false path. Note also that if different performance requirements are used, then different design parameters will be obtained.

A number of observations can be made from the obtained parameters. First, the markers for the design parameters were found to be the same as those computed in earlier studies [2]. Secondly, the error threshold is 0 in the search state but is 1 in the recovery verify states. This implies that the receiver should apply *hard decisions* in the search state to avoid locking on an incorrect marker. However, once it has located a possible marker it can apply *soft decisions* while raising the number of verifications. Thirdly, the error threshold exceeds 1 in the sync state and is 0 in the loss verify states. This implies that the receiver can apply *soft decisions* once it has attained synchronization but should apply *hard decisions* with more verification if a marker is received in error.

Table 1: Optimum design parameters for strategy A at $E = 2$

L	S	N	M	u_1	u_2	u_3	u_4
4	2	7	3	0	1	1	0
5	3	3	4	0	1	1	0
6	5	1	2	0	1	2	0
7	6	1	3	0	1	2	0
8	8	1	3	0	1	2	0
9	9	1	2	0	1	3	0
10	11	1	2	0	1	3	0
11	12	1	2	0	1	3	0
12	13	1	2	0	1	3	0
13	14	1	2	0	1	3	0
14	15	1	2	0	1	3	0

In order to give more light on the computed design parameters, we consider CCITT recommendation G.751 which employs FL = 2928 bits, $N = 3$, $M = 4$ and $u_1 = u_2 = u_3 = u_4 = 0$ [7]. This corresponds to $L = 12$ in Table 1. The modification proposed in [6] for this scheme is to use strategy B with $N = 3$, $M = 2$, $u_1 = 0$, $u_2 = 4$, $u_3 = 3$ and $u_4 = 4$. If strategy A is chosen, however, then we can use $N = 3$, $M = 2$, $u_1 = 0$, $u_2 = 2$, $u_3 = 4$ and $u_4 = 0$. The results for these two systems are given in Table 2. It is seen that

better performance is obtained by strategy A because the receiver will gain true synchronization (L_{14}) faster but will take longer to gain false synchronization (L_{15}). Also, the receiver will maintain true synchronization longer (L_{41}) but will lose false synchronization faster (L_{51}). Therefore, using strategy A gives better performance with lower values of u_2 (lowered from 4 to 2) and u_4 (lowered from 3 to 0).

Table 2: Performance parameters for strategies A and B for CCITT's G.751 recommendation at E = 3.

	Strategy A	Strategy B
L_{14} (frames)	4.4154	4.9392
L_{15} (frames)	0.7080E+48	0.1681E+45
L_{41} (frames)	0.4663E+36	0.3279E+34
L_{51} (frames)	3.4600	3.8802

CONCLUSION

The analysis of communication systems employing two strategies of *hard* and *soft decisions* has been performed. It has been found that the performance of the systems increase when some kind of *soft decision* is allowed during synchronization recovery as well as during loss of synchronization. It has been found, however, that the strategy employing *hard decisions* in the search and the loss verify states, and *soft decisions* in the sync and recovery verify states gives better performance. Optimum design parameters have also been computed for this strategy. The markers for these were found to be the same as those obtained for the *hard decision* systems analyzed in earlier reports. The recovery and loss verify numbers were found to be higher at lower frame lengths, and to stabilize to 1 and 2 respectively at higher frame lengths. The strategy proposed in this report has also been shown to have higher performance for the CCITT schemes than that proposed elsewhere.

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NOMENCLATURE

L_{14}	recovery time through the true path
L_{14}	recovery time through the false path
L_{41}	holding time through the true path
L_{51}	holding time through the false path
N	number of marker verifications during synchronization recovery
M	number of marker verifications during failure of synchronization
FL	frame length in bits = 2^L
l	lth bit in a frame
S	marker length in bits
R	number of data bits in a received S-bit word
P_e	probability that a received bit is in error
Q, P	transition probabilities between states
h	Hamming distance between received marker bits and receiver test bits
u	error threshold
T_1	time elapsed from when a receiver loses synchronization until it encounters the marker
T_2	time elapsed from when a receiver fails in an attempt to regain synchronization until the next encounter of the marker
T_s	time the receiver spends in synchronization
T_o	time the receiver spends out of synchronization
η	synchronization efficiency

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